US PAT NO: 6362023

DOCUMENT IDENTIFIER: US 6362023 B1
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TITLE: Dielectric based anti fuse cell with polysilicon contact plug and method for its manufacture

KWIC

Claims Text CLTX 7 :

7. A method for forming an anti fuse cell array comprising the steps of: providing a semiconductor substrate; forming a first insulating layer on the surface of the semiconductor substrate; forming a plurality of doped polysilicon (poly 1) lines on the insulating layer; forming a second insulating layer over the plurality of poly 1 lines; creating a **plurality of contact openings** through the second insulating layer and extending at least partially into the plurality of poly 1 **lines, the plurality of contact openings** exposing a portion of the plurality of poly 1 lines; forming a doped polysilicon plug layer on the second insulating layer and filling the **plurality of contact openings**; removing the doped polysilicon plug layer from the second insulating layer while leaving the doped polysilicon plug layer filling the **plurality of contact openings,** thereby forming a plurality of doped polysilicon contact plug; forming a dielectric layer on the second insulating layer and on the plurality of doped polysilicon contact plug; and forming a plurality if second doped polysilicon (poly 2) lines on the dielectric layer.

US PAT NO: 5635316

DOCUMENT IDENTIFIER: US 5635316 A
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TITLE: Layout methodology, mask set, and patterning method for phase shifting lithography

KWIC

Brief Summary Text BSTX 18 :
A method of producing a device layer layout is disclosed. A **plurality of lines** are defined, and the device features are placed on the lines. In this way, a phase edge or single edge feature mask can be produced from the layout to pattern an image corresponding to the lines. A second mask having the device features overlying the lines is also produced from the layout and is used to preserve wanted portions of the image and to remove unwanted portions of the image.

Detailed Description Text DETX 18 :
The present invention may be used to produce a layout to form small dimension openings in a photosensitive layer, which may be used to form, for example, contact or via openings. Referring to FIG. 9, a **plurality of contact openings** 901 are defined on the intersection of the plurality of vertical lines 920-927, and horizontal lines 930-936. As described earlier, the lines may be pre-defined or may be defined as the contacts are defined. In addition, the lines need not necessarily be periodic and need not necessarily be orthogonal as shown. In the embodiment shown herein, note that the

contacts are defined over intersections of the lines. As will be seen, this ensures that the phase edge layers and device feature layer may automatically be extracted from the database to produce the appropriate masks. Generally, it may be possible to use the same lines as those used for the layer to which contact is being made. Some additional lines may need to be defined in the contact layer to produce intersections at each contact opening, where, for example, a contact overlies a portion of an underlying line not at an intersection. For example, referring back to FIG. 5, if it were desired to contact line 503, it would be necessary to add a line intersecting line 524 at some point along line 524 where feature 503 is present to produce an intersection. Furthermore, the contact layer need not necessarily have all the lines of the underlying layer, as the underlying layer typically has a greater density of features than the contact layer.

Detailed Description Text - DETX (22) :

Next, the photosensitive layer is exposed to a mask having the features 901 disposed at those intersections where contact openings are desired. After this exposure and development, contact openings will be present as shown in FIG. 12, as all other regions of the photoresist layer are substantially exposed in one or more of the above described three exposures. Again, it will be appreciated that the masks 1000, 1100, and the mask having the features 901 may be exposed in any order. As shown in FIG. 13, a **plurality of contact openings** 1301 are formed in the photosensitive layer in the regions underneath the features 901. Again, only some of the contact openings 1301 are labeled for clarity.

Detailed Description Text - DETX 26 :

As described herein, the present invention comprises defining a **plurality of lines** which, depending upon the features, may be arranged in rows and/or columns. The definition of the lines may be done in a variety of manners. In one embodiment, lines may be pre-defined with respect to the earlier described grid points in relation to which features are typically defined. For example, in one embodiment the lines may be laid out in rows and columns spaced at approximately the minimum pitch. Features can then be placed on these lines as they are encountered by the system. Alternatively, lines can be defined as features are created. In this embodiment, it should be ensured that no two lines are spaced closer than approximately the minimum pitch, although lines may be placed apart greater than the minimum.

Claims Text CLTX 6 :

defining said **plurality of lines**;

US PAT NO: 6465298

DOCUMENT IDENTIFIER: US 6465298 B2
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TITLE: Method of fabricating a semiconductor on insulator memory cell with buried word and body lines

KWIC

Brief Summary Text BSTX 14 :

Another embodiment of the present invention provides a semiconductor memory device, including a memory array. The memory array includes a plurality of bit **lines, a plurality** of word **lines, and a plurality** of memory cells. Each memory cell includes an access transistor having a gate region, a body region, and first and second source/drain regions. Each memory cell includes a storage capacitor that is electrically coupled to the second source/drain region of the access transistor. Access circuitry is provided for accessing the memory cells. A plurality of isolation trenches is provided, including a first trench between first and second access transistors and a second trench between the second and third access transistors. A first one of the word lines is located in the first trench at a height that is no higher than the upper surface of the access transistor. The first word line is electrically coupled to the gate regions of the first and second access transistors. A first one of the body lines is located in the second trench at a height that is no higher than the upper surface of the access transistor. The first body line is electrically

coupled to the body portions of the second and third access transistors. A
first one of the bit lines is coupled to the first source/drain region of each
of the first, second and third access transistors.

Claims Text CLTX 8 :
8. The method of claim 1, including: interposing an insulating layer
between the body line and the second trench; forming a **plurality of contact**
openings through the insulating layer between the body line and the body
regions of the access transistors; and forming contacts in the contact
openings for electrically coupling the body line and the body regions of the
access transistors.

Claims Text CLTX 20 :
20. A method of fabricating a memory array on a semiconductor substrate,
comprising: forming at least first and second trenches in the substrate to
define a bar of semiconductor material; forming an insulating layer between
the bar and the substrate for providing electrical isolation therebetween;
defining a plurality of active areas of semiconductor material on the bar;
producing an access transistor in each of the active areas, each access
transistor including gate, body, and first and second source/drain regions;
forming a buried word line; coupling the word line to the gate region of at
least one of the access transistors; forming a buried body line; electrically
connecting the body line to the body region of at least one of the access
transistors; forming a **plurality of contact openings** through an insulating
layer between the buried body line and the body regions of the access
transistors; and forming contacts in the contact openings for electrically

coupling the buried body line and the body regions of the access transistors.